What is Claimed is:

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1. A digital processing system having a microprocessor, wherein the microprocessor comprises:

fetch circuitry for fetching instruction fetch packets, wherein each fetch packet contains a first plurality of instructions;

a second plurality of functional units, the plurality of functional units operable to execute a second plurality of instructions in parallel, and

dispatch circuitry operable to select an execution packet from one or more fetch packets, wherein an execute packet varies in size and contains only a set of instructions that can be executed in parallel on the plurality of functional units, whereby a first execute packet contains a different number of instructions than a second execute packet due to resource constraints.

2. The digital processing system of Claim 1, wherein the first plurality is equal in number to the second plurality.

3. The digital processing system of Claim 1, wherein a first execute packet spans a first fetch packet and a second fetch packet.

4. The digital system of Claim 3, wherein the dispatch circuitry comprises:

a first latch to hold the first fetch packet;

a second latch to hold the second fetch packet;

selection circuitry to select a first portion of the first execute packet from the first latch and a second portion of the first execute packet from the second latch.

5. The digital system of Claim 4, wherein the dispatch circuitry further comprises control circuitry connected to a plurality of instruction positions corresponding to the plurality of instructions of a fetch packet in the first latch and in the second latch to determine a boundary of each execute packet, the control circuitry operable to control the selection circuitry in response to an execute packet boundary.

6. The digital system according to Claim 5 being a cellular telephone, further comprising:

an integrated keyboard connected to the processor via a keyboard adapter;

a display, connected to the processor via a display adapter;

radio frequency (RF) circuitry connected to the processor; and

an aerial connected to the RF circuitry.

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7. A method of operating a digital system having a microprocessor, wherein the microprocessor has a plurality of functional units for executing instructions in parallel, comprising the steps of:

fetching a sequence of instruction fetch packets, wherein each fetch packet contains a first plurality of instructions;

examining each fetch packet to determine an execution packet boundary;

selecting a first portion of an execute packet from a first fetch packet and a second portion of a first execute packet from a second fetch packet if the first execute packet boundaries span the first fetch packet and the second fetch packet.

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